REMARKS

Claims 1, 2, and 5-12 stand rejected under § 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA), in view of Shimomaki (U.S. Patent No. 7,221,344). Applicant respectfully traverses this rejection for the reasons below.

With regard to independent claim 1, Applicant traverses the rejection because AAPA and Shimomaki, taken alone or in combination, do not disclose or suggest that a gate signal is raised in the main scanning at a timing on after a first inversion of the data scanning signal occurring during the selected horizontal scanning period, and that the gate signal is broken down in the main scanning at a timing prior to the next following inversion of the data signal occurring during the selected horizontal scanning period.

The Examiner recognizes that AAPA is silent regarding this feature, but cites the "n-th FIELD" in Fig. 9 of Shimomaki as corresponding to the selected horizontal scanning period recited in claim 1. However, a field period is different from a horizontal scanning period. An active matrix type liquid crystal display panel has a plurality of gate lines, which are generally scanned sequentially. In Shimomaki, one field period is the period in which all gate lines are scanned. In contrast, one horizontal scanning period is the period in which one gate line is scanned. Thus, one field period includes a plurality of horizontal scanning periods (see the marked-up reproduction of Fig. 9 of Shimomaki below). Therefore, Shimomaki fails to disclose or suggest the claimed features of the gate signal as described in claim 1. Accordingly, even if combined, AAPA and Shimomaki still would not

disclose or suggest these features. For this reason, claim 1 and its associated dependent claims are allowable over the cited references.

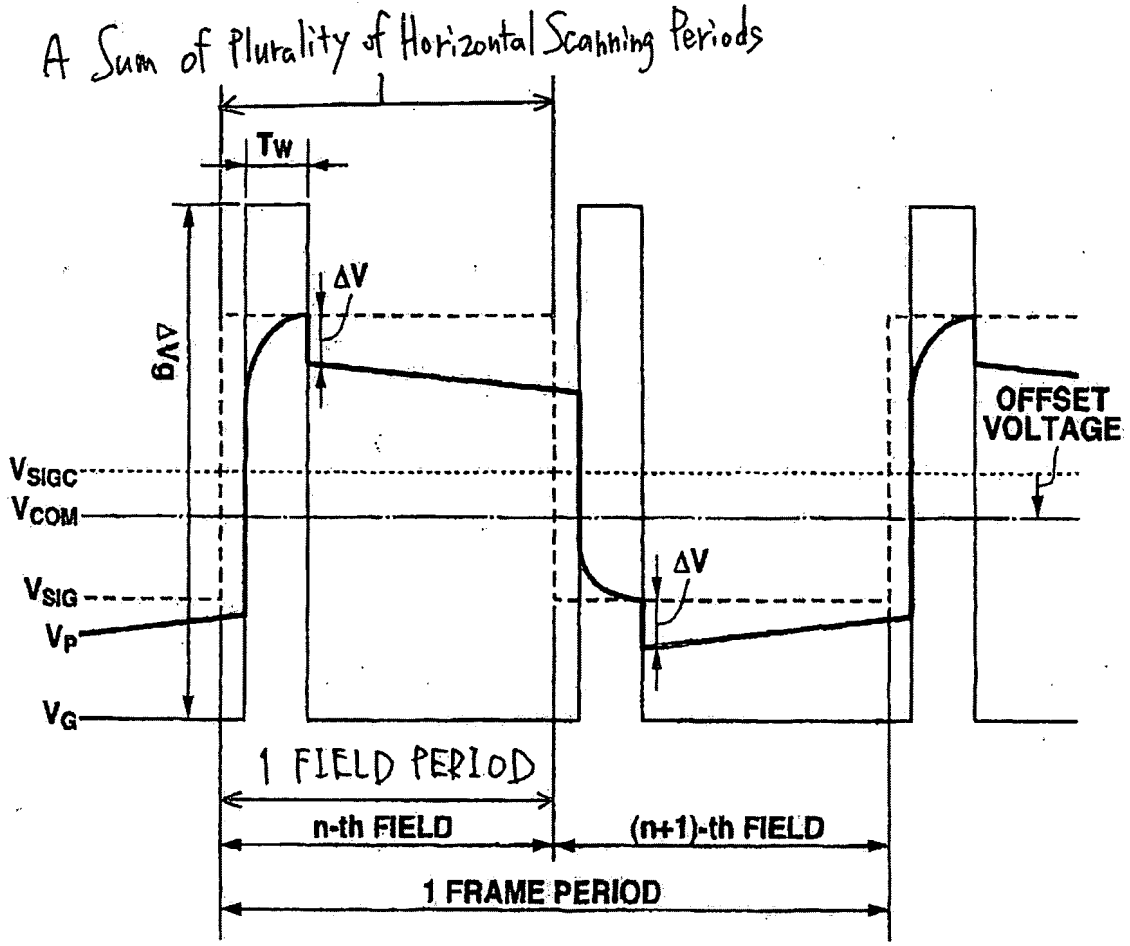


FIG.9

Regarding independent claim 5, Applicant traverses the rejection because AAPA and Shimomaki fail to disclose or suggest that a value of the predetermined pre-writing data voltage that is the data voltage in the pre-writing data voltage period is different from a value of a display data voltage that is the data voltage in the another period.

As shown, for example, in Fig. 9 of the present Application, a horizontal scanning period includes a pre-writing data voltage period C, and another period A. During the pre-writing data voltage period C of the horizontal scanning period, the value of a data signal 29 is reduced, relative to a value of the data signal 29 in the period A. Put another way, the value of the data signal 29 is lower during the pre-writing data voltage period C than the value of the same signal during period A

In contrast, AAPA shows in Fig. 27, a horizontal scanning period A, during which main scanning occurs, and another period B. Pre-scanning occurs during period B. The value of a data signal 10 during the pre-scanning period B is the same as the value of the data signal during the main scanning period A. Thus, Fig. 27 does not show a value of a pre-writing data voltage (i.e., a data voltage in the pre-writing data voltage period of the horizontal scanning period) that is different from a value of a display data voltage in another period of the horizontal scanning period. Accordingly, AAPA does not disclose or suggest that a value of the pre-writing data voltage that is the data voltage in the pre-writing data voltage period is different from a value of a display data voltage that is the data voltage in the another period.

Shimomaki is directed to a liquid crystal display device and driving control method thereof. The Examiner does not rely on Shimomaki to disclose any of the features of claim 5. Therefore, even if Shimomaki were combined with AAPA, the references still would not disclose or suggest that a value of the pre-writing data voltage that is the data voltage in the pre-writing data voltage period is different from a value of a display data

voltage that is the data voltage in the another period. For this reason, Applicant asserts that claim 5 and its associated dependent claims are allowable over the cited references.

Regarding claim 11, Applicant traverses because AAPA and Shimomaki, fail to disclose or suggest that a value of a gate-off voltage between the pre-scanning period and the main scanning period is higher than a value of the gate-off voltage after the main scanning period. In the present invention, as shown in Fig. 8, a gate signal 28 is raised to a gate-on voltage with a value of 30V during a pre-scanning period B. After the pre-scanning period B, the gate signal 28 is lowered to a gate-off voltage with a value of 0V between the pre-scanning period B and a main scanning period A. Then, the gate signal 28 is returned to the gate-on voltage of 30V during the main scanning period A. After the main scanning period A, the gate signal 28 is lowered to an even lower gate-off voltage, having a value of -5V. Thus, the gate-off voltage between the pre-scanning period B and the main scanning period A is higher than the gate-off voltage after the main scanning period.

In contrast, AAPA shows in Figs. 26-28, a gate signal that fluctuates between a gate-off value and a gate-on value. The gate signal rises to the gate-on value during a pre-scanning period B and a main scanning period A, and otherwise remains at the gate-off value. As is clearly shown in each of the figures, the value of the gate-off voltage between the pre-scanning period B and the main scanning period A is the same as the value of the gate-off voltage after the main scanning period. Therefore, AAPA fails to disclose or suggest a value of a gate-off voltage between the pre-scanning period and the main scanning period

that is higher than a value of the gate-off voltage after the main scanning period, as described in claim 11.

As described above, Shimomaki is directed to a liquid crystal display device and driving control method thereof. The Examiner does not cite Shimomaki to disclose any of the features of claim 11. Therefore, AAPA and Shimomki, taken alone or in combination, do not disclose or suggest that a value of a gate-off voltage between the pre-scanning period and the main scanning period is higher than a value of the gate-off voltage after the main scanning period. Accordingly, Applicant respectfully requests the withdrawal of this rejection of Claim 11.

Claims 3 and 4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Yasukatsu et al. (JP Pub. No. 09-274170). Applicant traverses this rejection for the reasons below.

With respect to claim 3, Applicant traverses the rejection because AAPA and Yasukatsu fail to disclose or suggest that a value of an on-voltage of a gate signal in the pre-scanning is different from the value of an on-voltage of the gate signal in the main scanning. Fig 19 shows a schematic of a major portion of a liquid crystal display device according to the present invention. Here, an internal voltage-generating circuit 30 outputs signal Vgon1 and Vgon2 to a gate-on voltage changeover circuit 32. Vgon1 and Vgon2 represent different voltage values to be output. For example, the value of voltage Vgon1 may be 20V, and the value of voltage Vgon2 may be 30V.

Signals Vgon1 and Vgon2 are then used as gate voltages during a pre-scanning period and main scanning period, as shown in Figs. 21-23 of the present Application. For example, Fig. 21 shows that a value of a gate-on voltage used during pre-scanning Vgon1 is lower than a value of a gate-on voltage used during main scanning Vgon2. Fig 22 shows that the value of a gate-on voltage Vgon2 used during the pre-screening period may also be higher than a value of the gate-on voltage Vgon1 used during the main scanning period. Thus, in the present invention, the value of a gate-on voltage of the gate signal in the pre-scanning period is different than the value of the gate-on voltage of the gate signal in the main scanning period.

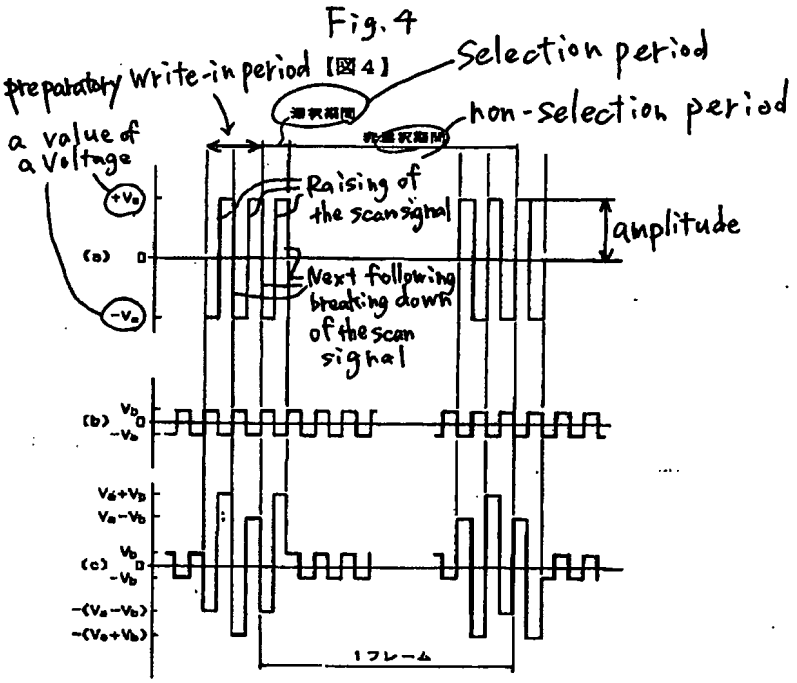
The Examiner asserts that AAPA shows, in Figs. 26-28, that the value of the on-voltage during the pre-scanning period is different from the value of the on-voltage during the main scanning period. However, this is simply not the case. Figs 26-28 clearly show that the value of a gate-on voltage of gate signal 12 is the same during both a pre-scanning period B and a main scanning period A.

Yasukatsu, which is directed to a liquid crystal display, is not cited by the Examiner as disclosing any of the features of claim 3. Accordingly, even if Yasukatsu were combined with AAPA, the references still would not disclose or suggest that a value of an on-voltage of a gate signal in the pre-scanning is different from the value of an on-voltage of the gate signal in the main scanning. For this reason, claim 3 is allowable over the cited references.

Regarding claim 4, Applicant traverses the rejection because AAPA and Yasukatsu fail to disclose or suggest a length of time between a time of raising a gate signal and a time of a next following breaking down of the gate signal in the pre-scanning period is different from that in the main scanning period.

As shown in Figs. 2-4, 7-9, 11-15, 17 and 21-23 of the Application, for example, the amount of time between the raising of a gate signal and the next following lowering of the gate signal in a pre-scanning period is different than the amount of time between the raising of a gate signal and the next following lowering of the gate signal in a main scanning period.

The Examiner acknowledges that AAPA does not teach this feature, but asserts that Yasukatsu discloses a length of time between a time of raising a gate signal and a time of a next following breaking down of the gate signal in the pre-scanning period is different from that in the main scanning period. Applicant respectfully disagrees. As shown in Fig. 4(a) of Yasukatsu (reproduced with notations below), a length of time between a time of raising a scan signal (which corresponds to a gate signal of the present invention) and a time of a next following breaking down of the scan signal in the preparatory write-in period (i.e., the pre-scanning period) is the same as that in the selection period (i.e., the main scanning period).



Therefore, Yasukatsu and AAPA, taken alone or in combination, fail to disclose or suggest the features of claim 4. For this reason, Applicant respectfully requests withdrawal of the rejection of claim 4.

For all the foregoing reasons, Applicant submits that this Application is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

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January 25, 2008

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